Notice of Allowability	Application No.	Applicant(s)	
	10/002,987	DAI ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the request for reconsdieration filed on 20 September 2004*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☒ The drawings filed on *03 November 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 20 September 2004. Claims 1-25 are pending; claims 8-25 have been previously allowed.

Allowable Subject Matter

Claims 1-25 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of forming shallow trench isolation regions in the manufacture of an integrated circuit device where an etch stop layer is deposited on the surface of a semiconductor substrate; etching a plurality of isolation trenches through semiconductor substrate whereby narrow active areas and wide active areas of the semiconductor substrate are left between the isolation trenches; depositing an oxide layer over the etch stop layer and within the isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after the oxide layer fills the isolation trenches, the deposition component is discontinued while continuing the sputtering component until the oxide layer is at a desired depth in the isolation trenches whereby the oxide layer within the isolation trenches is disconnected from the oxide layer overlying the etch stop layer; thereafter etching away the oxide layer overlying the etch stop layer in the wide

active areas wherein oxide layer residues are left overlying the etch stop layer; and removing the etch stop layer and the oxide residues to complete planarized the shallow trench isolation regions in the manufacture of the integrated circuit device.

For example, Lee (6,197,691) discloses a method of forming shallow trench isolation regions where a silicon nitride etch stop layer (34) in deposited using a chemical vapor process (CVD) on to a semiconductor substrate (30); etching a plurality of isolation trenches (Fig. 6) through the silicon nitride etch stop layer (34) into the semiconductor substrate (30), whereby narrow active areas and wide active areas of the semiconductor substrate (30) are left between the isolation trenches; depositing an oxide layer (38) over the silicon nitride etch stop layer (34) and within the isolation trenches using a high density plasma chemical vapor deposition (HDP-CVD); etching away the oxide layer (38) overlying the silicon nitride etch stop layer (34) and then removing the silicon nitride etch stop layer (34). Lee further discloses the silicon nitride etch stop layer (34) having a thickness between 1500 and 2500 Angstroms, and the removing the silicon nitride etch stop layer (34) with a hot phosphoric acid (H_3PO_4) dip (col. 3, lines 38-65; col. 4, lines 59-65). However, Lee does not disclose, anticipate, teach, or suggest depositing an oxide layer over the etch stop layer and within the isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after the oxide layer fills the isolation trenches, the deposition component is discontinued while continuing the sputtering component until the oxide layer is at a desired depth in the isolation trenches whereby the oxide layer within the isolation trenches is

disconnected from the oxide layer overlying the etch stop layer; thereafter etching away the oxide layer overlying the etch stop layer in the wide active areas wherein oxide layer residues are left overlying the etch stop layer.

Lim et al. (6,403,484) disclose a method of forming shallow trench isolation regions in the manufacture of an integrated circuit device where an etch stop layer (14) is deposited on the surface of a semiconductor substrate (10); etching a plurality of isolation trenches (15) through semiconductor substrate (10) whereby narrow active areas and wide active areas of the semiconductor substrate (10) are left between the isolation trenches (15) (Fig. 1; col. 2, lines 51-62); depositing an oxide layer (16) over the etch stop layer (14) and within the isolation trenches (15) using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after the oxide layer (16) fills the isolation trenches (15), the deposition component is discontinued while continuing the sputtering component until the oxide layer (16) is at a desired depth in the isolation trenches (15) whereby the oxide layer (20) within the isolation trenches (15) is disconnected from the oxide layer (18) overlying the etch stop layer (14) (Fig. 3; col. 3, lines 4-35); and removing the etch stop layer (14) and the oxide layer (18) to complete planarized the shallow trench isolation regions in the manufacture of the integrated circuit device (Fig. 7; col. 3, lines 43-59). However, Lim et al. do not disclose, anticipate, teach or suggest etching away the oxide layer overlying the etch stop layer in the wide active areas wherein oxide layer residues are left overlying the etch stop layer. Also, Lim et al. is commonly assigned to the present invention.

The prior art made of record in this action does not anticipate, teach, or suggest a method of forming shallow trench isolation regions in the manufacture of an integrated circuit device where an etch stop layer is deposited on the surface of a semiconductor substrate; etching a plurality of isolation trenches through semiconductor substrate whereby narrow active areas and wide active areas of the semiconductor substrate are left between the isolation trenches; depositing an oxide layer over the etch stop layer and within the isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after the oxide layer fills the isolation trenches, the deposition component is discontinued while continuing the sputtering component until the oxide layer is at a desired depth in the isolation trenches whereby the oxide layer within the isolation trenches is disconnected from the oxide layer overlying the etch stop layer; thereafter etching away the oxide layer overlying the etch stop layer in the wide active areas wherein oxide layer residues are left overlying the etch stop layer; and removing the etch stop layer and the oxide residues to complete planarized the shallow trench isolation regions in the manufacture of said integrated circuit device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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